REMARKS

This amendment is responsive to the Office Action dated July 22, 2005. Applicants have amended claims 39-42, 46, 47, 50-54 and 58-62. Claims 39-79 remain pending.

Claim Objection

In the Office Action, the Examiner objected to claims 39-42, 46, 47, 51-54 and 58-62 for use of the phrase "adapted to". The Examiner asserted that use of this phrase is optional language according to MPEP 2106.II.C. Applicants have amended claims 39-42, 46, 47, 51-54 and 58-62 to remove the phrase "adapted to" as requested by the Examiner. Applicants request withdrawal of the objection.

Claim Rejection Under 35 U.S.C. § 112

In the Office Action, the Examiner rejected claims 50 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants have amended claim 50 for purposes of clarification. Claim 50 now recites an output port coupled to said multiple entry point FIFO to receive said data from said *multiple entry point FIFO* and transmit said data on a communications link. Applicants submit that claim 50, as amended, particularly point out and distinctly claim the subject matter, as required by 35 U.S.C. 112, second paragraph.

Claim Rejection Under 35 U.S.C. § 102

Claim 39

In the Office Action, the Examiner rejected claim 39 under 35 U.S.C. 102(e) as being anticipated by Dai et al. (USPN 6,658,016). Applicants respectfully traverse the rejection. Dai et al. (Dai) fails to disclose each and every feature of the claimed invention, as required by 35 U.S.C. 102(e), and provides no teaching that would have suggested the desirability of modification to include such features.

For example, Dai et al. fails to teach or suggest an apparatus comprising request logic coupling a *set* of input ports to a FIFO storage buffer, and a memory in communication with said request logic, wherein the memory concurrently maintains a plurality of pointers, wherein each

pointer corresponds to a different location in the *FIFO storage buffer* for storing data from an input port in the set of input ports, as recited by Applicants' independent claim 39.

Applicants describe an apparatus (e.g., a cross-bar switch) that includes a plurality of input ports, a plurality of sink ports, and a plurality of data rings in communication with the plurality of input ports and the plurality of sink ports. Each of the sink ports includes a plurality of inputs, a first-in-first-out (FIFO) storage buffer, and request logic that couples the plurality of inputs to the FIFO storage buffer. The request logic stores data received from each of the plurality of input ports in the same FIFO storage buffer. A memory stores a plurality of pointers, each of which corresponds to a different location in the FIFO storage buffer. The FIFO storage buffer stores data received from the plurality of input ports in a sequential manner such that the order in which the data is stored in the FIFO storage buffer is the same order in which the data is read from the FIFO storage buffer. In this way, the FIFO serves as a staging area for accumulating packet data for transmission onto a communications link.[1]

Dai describes a switch in which one of a plurality of input ports (88) receives a data packet and a packet control unit (340) coupled to the plurality of input ports stores the data packet in a *packet buffer* (100). Dai also describes a memory unit within the packet buffer control unit (340) for storing pointer address location information associated with each of the data packets stored in the packet buffer (100).[2] However, the packet buffer (100) described by Dai is not a FIFO storage buffer. Instead, Dai teaches that the packet buffer control (340) is responsive to channel data transfer signals and operative to read a *selected* data packet indicated by the packet location pointer information from the packet buffer (100).[3] Dai never suggests that the data packets stored in the packet buffer (100) are stored in a sequential manner such that the data packets are read from the buffer in the same order in which the data packets were stored in the buffer, as required by a FIFO storage buffer.

Furthermore, Dai describes a FIFO storage buffer (330) coupled to the packet buffer (100). Dai states that a packet routing control unit (302) is operative to append data bursts, provided by the packet buffer 100 via the FIFO 330, with block header information.[4] Thus, the

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[1] *Applicants*, Page 21, ll. 30-31.
[2] *Dai et al.*, Col. 13, ln. 30 – Col. 14, ln. 11.
[3] *Dai et al.*, Col. 15, ll. 18-35.
[4] *Dai et al.*, Col. 14, ll. 64-67.

only manner in which data is added to FIFO (330) is by appending the data stored in the packet buffer (100). In this manner, the FIFO (330) described by Dai has only a single data input from the packet buffer (100). Dai fails to teach or suggest the FIFO (330) having a *set* of input ports, as recited by Applicants' claim 39. In addition, Dai does not mention request logic concurrently maintaining a plurality of pointers corresponding to locations in the *FIFO storage buffer.* As described above, Dai merely describes the packet buffer control (340) storing pointer information for locations in the packer buffer (100), which is not a FIFO buffer and does not function like a FIFO buffer. Dai fails to describe a *FIFO storage buffer* that stores data from the set of input ports and a memory that concurrently maintains a plurality of pointers corresponding to different locations in the FIFO for storing the data.

Dai also fails to teach or suggest an apparatus comprising request logic that *simultaneously* writes data to the FIFO storage buffer for at least two of the input ports, as recited by Applicants' amended independent claim 39. As described above, Dai does not describe the request logic coupling the set of input ports to the FIFO storage buffer. The FIFO (330) disclosed by Dai has only one data input. Dai does not disclose the request logic writing data to the FIFO storage buffer for at least two of the input ports, let alone *simultaneously* writing the data for the at least two input ports.

Dai fails to disclose each and every limitation set forth in claim 39. For at least these reasons, the Examiner has failed to establish a prima facie case for anticipation of Applicants' claim 39 under 35 U.S.C. 102(e). Withdrawal of this rejection is requested.

Claims 39-66, 71 and 72

In the Office Action, the Examiner rejected claims 39-66, 71 & 72 under 35 U.S.C. 102(e) as being anticipated by Mann et al. (USPN 6,212,165). Applicant respectfully traverses the rejection. Mann et al. (Mann) fails to disclose each and every feature of the claimed invention, as required by 35 U.S.C. 102(e), and provides no teaching that would have suggested the desirability of modification to include such features.

Regarding Applicants' amended independent claim 39, Mann fails to teach or suggest an apparatus comprising request logic that couples a set of input ports to a FIFO storage buffer,

wherein the request logic *simultaneously* writes data to the FIFO storage buffer for at least two of the input ports.

Applicants disclose an apparatus (e.g., a cross-bar switch) that includes a plurality of input ports, a plurality of sink ports, and a plurality of data rings in communication with the plurality of input ports and the plurality of sink ports. Each of the sink ports includes a plurality of inputs and a multiple entry point first-in-first-out (FIFO) storage buffer. The multiple entry point FIFO includes request logic that *simultaneously* writes multiple data packets for at least two of the plurality of input ports to the FIFO storage buffer. The ability to simultaneously write multiple packets enables a sink port's non-blocking operation.[5] Furthermore, Applicants describe the FIFO storage buffer as a multiple port memory capable of simultaneously performing data exchanges on multiple ports. In this manner, there is no need to arbitrate access to the FIFO storage buffer as the request logic can directly transfer data to the FIFO storage buffer.[6]

On the contrary, Mann describes a port combiner (30) that writes data from a plurality of external ports (12) to a FIFO queue (36) by continuously scanning all the external ports (12) in a round robin fashion looking for a port with data ready to be input. If an external port has data read to be input, the port combiner (30) pumps the data from the port to the controller (34). The controller (34) in turn writes the input data into the FIFO queue (36). Mann makes no mention of *simultaneously* writing data to the FIFO storage buffer for at least two of the input ports. Instead, Mann describes a data input scheme that provides a period of time to receive data from each of the external ports separately. The system described by Mann is not capable of simultaneously writing data for two or more input ports to a FIFO storage buffer, as recited by Applicants' amended claim 39.

In a similar manner, Mann fails to teach or suggest an apparatus comprising request logic that couples a set of input ports to a FIFO storage buffer, wherein the request logic *simultaneously* writes data to the FIFO storage buffer for at least two of the input ports, as recited by Applicants' amended independent claim 46.

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[5] *Applicants*, Page 4, ll. 25-29.
[6] *Applicants*, Page 22, ll. 7-13.

As described above, Applicants disclose an apparatus (e.g., a cross-bar switch) that includes a plurality of sink ports, each of the sink ports including a plurality of inputs and a multiple entry point first-in-first-out (FIFO) storage buffer. The multiple entry point FIFO includes request logic that *simultaneously* writes multiple data packets for at least two of the plurality of input ports to the FIFO storage buffer. Mann fails to teach this feature of Applicants claimed invention. Instead, Mann describes a port combiner (30) that writes data from a plurality of external ports (12) to a FIFO queue (36) by continuously scanning all the external ports (12) in a round robin fashion looking for a port with data ready to be input. Mann makes no mention of *simultaneously* writing data to the FIFO storage buffer for at least two of the input ports.

In regard to Applicants' amended independent claim 50, Mann fails to teach or suggest a *sink port* comprising a multiple entry point FIFO having a plurality of data inputs in communication with a set of input ports, and an output port coupled to said *multiple entry point FIFO* to receive the data from the multiple entry point FIFO and transmit the data on a communications link.

In the Office Action, the Examiner erroneously asserted that Mann teaches a *sink port* comprising a plurality of data inputs and a multiple entry point FIFO. The Examiner has provided no support from Mann, or any other prior art of record, that describes a sink port including a multiple entry point FIFO having plurality of data inputs, and an output port, as recited by Applicants' claim 50. In fact, Mann makes no mention of the disclosed system (70) being a sink port. Instead, Mann describes the system (70) illustrated in FIG. 2 as a portion of a network device, such as a switch. Mann fails to suggest that the plurality of external ports (12) and the multiple input FIFO queue (10) are included within a sink port.

Furthermore, the Examiner stated that Mann discloses an output port (external ports 12) coupled to the FIFO to receive data from a storage buffer (40) and transmit data on a communication link (resources). In this way, the Examiner has defined the plurality of data inputs and the output port as the same component, i.e., external ports 12. The Examiner's characterization of this portion of Applicants' invention is incorrect. Applicants' claim 50 recites a sink port including the separate components of a multiple entry point FIFO having a plurality of data inputs and a single output port coupled to the multiple entry point FIFO.

Regardless, Mann fails to describe a single output port within a sink port that receives data directly from the multiple entry point FIFO and transmits the data on a communications link. Mann does not disclose an output port coupled to the multiple input FIFO. Instead, Mann teaches that the data read out of the FIFO queue (36) is placed into another buffer (40) by the controller (34). The buffer (40) then performs rate adaptation between the FIFO queue (36) and the switch fabric (42).[7] Mann makes no mention of an output port that receives data directly from the *multiple entry point FIFO*, as recited by amended claim 50.

Regarding Applicants' independent claim 58, Mann fails to teach or suggest a cross-bar switch comprising a set of input ports and a set of sink ports in communication with said set of input ports, wherein a first sink port in said set of sink ports includes a multiple entry point FIFO having a plurality of data inputs that store data from data packets accepted by said first sink port.

In support of the rejection, the Examiner asserted that Mann teaches a set of sink ports (10) in communication with the set of input ports (12) and a multiple entry point FIFO (10) having a plurality of data inputs to store data from data packets. Applicants are confused by the Examiner's assertion. It is unclear to Applicants how the FIFO queue 10 described in the Mann reference can comprise both a set of sink ports *and* a multiple entry point FIFO. As described above, Mann makes no mention of the disclosed system (70) being a sink port. Mann also makes no mention of the disclosed multiple input FIFO queue (10) being a sink port.

Furthermore, the Examiner failed to consider that *each* sink port in the set of sink ports includes a multiple entry point FIFO. Even if the multiple input FIFO (10) described by Mann could be considered a sink port, Mann would not disclose each and every feature of Applicants' claimed invention. Mann fails to teach or suggest a *set* of sink ports wherein each sink port in the set of sink ports comprises a multiple entry point FIFO, as recited by Applicants claim 58.

Mann also fails to teach or suggest a method for a *sink port* in a cross-bar switch to collect data in a FIFO comprising the steps of accepting data from a first data packet, wherein said accepted data is a *subset* of said first data packet, storing the first subset data in said FIFO, accepting data from a second data packet, wherein said accepted data is a *subset* of said second data packet, and storing the second subset data in said FIFO, as recited by Applicants' independent claim 71. The Examiner again erroneously asserted that Mann teaches the features

[7] *Mann et al.*, Col. 5, ll. 6-13.

of Applicants' claim 71. As described above, Mann does not describe a *sink port* in a cross-bar switch collecting data in a FIFO. Mann fails to make any mention of the disclosed system (70) or the disclosed multiple input FIFO (10) being a sink port.

In addition, the Examiner did not consider the feature recited by Applicants' claim 71 of accepting data from a data packet when the data is a *subset* of the data packet. Regardless, Mann fails to disclose or suggest accepting data from a data packet that is a *subset* of the data packet. Col. 4, lines 53-65 of Mann clearly state that if an external port has data ready to input, the port combiner (30) pumps the data from the external port to the controller (34), which in turn writes the input data into the FIFO queue (36). Nowhere does Mann mention accepting data from a data packet that is only a *subset* of the data packet.

For at least the reasons described above in reference to Applicants' independent claims 39, 47, 50, 58 and 71, Applicants' dependent claims 40-46, 48-49, 51-57, 59-70 and 72-79 are also in condition for allowance.

In order to support an anticipation rejection under 35 U.S.C. 102(e), it is well established that a prior art reference must disclose each and every element of a claim. This well known rule of law is commonly referred to as the "all-elements rule."[8] If a prior art reference fails to disclose any element of a claim, then rejection under 35 U.S.C. 102(e) is improper. [9]

Mann fails to disclose each and every limitation set forth in claims 39-66, 71 and 72. For at least these reasons, the Examiner has failed to establish a prima facie case for anticipation of Applicants' claims 39-66, 71 and 72 under 35 U.S.C. 102(e). Withdrawal of this rejection is requested.

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[8] *See Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81 (CAFC 1986) ("it is axiomatic that for prior art to anticipate under 102 it has to meet every element of the claimed invention").
[9] *Id. See also Lewmar Marine, Inc. v. Barient, Inc.* 827 F.2d 744, 3 USPQ2d 1766 (CAFC 1987); *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (CAFC 1990); *C.R. Bard, Inc. v. MP Systems, Inc.*, 157 F.3d 1340, 48 USPQ2d 1225 (CAFC 1998); *Oney v. Ratliff*, 182 F.3d 893, 51 USPQ2d 1697 (CAFC 1999); *Apple Computer, Inc. v. Articulate Systems, Inc.*, 234 F.3d 14, 57 USPQ2d 1057 (CAFC 2000).

Claim Rejection Under 35 U.S.C. § 103

In the Office Action, the Examiner rejected claims 67-70 & 73-76 under 35 U.S.C. 103(a) as being unpatentable over Mann in further view of Dai. Applicant respectfully traverses the rejection. The applied references fail to disclose or suggest the inventions defined by Applicant's claims, and provide no teaching that would have suggested the desirability of modification to arrive at the claimed invention.

With reference to dependent claims 67-70, for example, the applied references lack any teaching that would have suggested a cross-bar switch having set of data rings in communication with said set of input ports and said set of sink ports of that cross-bar switch. Furthermore, both Mann and Dai, either singularly or in combination, fail to describe a cross-bar switch, as recited by Applicants' independent claim 58 from which claims 67-70 depend.

The Examiner correctly acknowledged that Mann fails to disclose a cross-bar switch having a set of data rings in communication with said set of input ports and said set of sink ports of that cross-bar switch. However, the Examiner asserted that Dai discloses a cross-bar switch having a set of data rings in communication with a set of input ports and a set of output ports of that switch. On the contrary, Dai fails to describe *a cross-bar switch* having a set of data rings in communication with the set of input ports and the set of sink ports *within the cross-bar switch*. Instead, Dai describes a packet switching fabric in which a plurality of switching devices are coupled in a ring fashion. The Dai switch fabric is properly viewed as a ring of switches. For example, FIG. 1 of Dai illustrates four distinct switching devices 12 coupled in a ring-like manner using an external data ring 18 and a control ring 24. The data ring 18 includes a plurality of data ring segments each coupling a corresponding adjacent pair of the devices together to ultimately form a ring.

In contrast, Applicants describe and claim a single cross-bar switch in which the cross-bar switch itself includes data rings for transferring packets directly between the input ports and the output (sink) ports of that same cross-bar switch. For purposes of clarity, Applicants refer the Examiner to Figure 2 of the present application that illustrates exemplary internal architecture of Applicants' described cross-bar switch. When properly viewed, the Dai switches that may be connected to form a "ring" are fundamentally different from the internal apparatus architecture described and claimed by the Applicants. Dai fails to teach or suggest that the internal

architecture of any of the switches comprises a ring topology that connects the input ports and the output ports within the individual switch. Thus, the Examiner is incorrect when asserting that Dai teaches a cross-bar switch comprising a set of input ports to receive data packets, a set of sink ports in communication with said set of input ports to receive and forward said data packets, and a set of data rings in communication with said set of input ports and said set of sink ports.

With reference to dependent claim 73, the applied references lack any teaching that would have suggested determining that the first subset data accepted from the first data packet includes a *first line* of said first data packet and determining that the second subset data accepted from the second data packet includes a *first line* of said second data packet. Furthermore, both Mann and Dai, either singularly or in combination, fail to describe a method for a sink port in a cross-bar switch to collect data in a FIFO, as recited by Applicants' independent claim 71 from which claim 73 depends.

The Examiner correctly acknowledged that Mann fails to disclose determining that the data accepted from the data packet includes a first line and allocating a location in the FIFO for storing data from the data packet. However, the Examiner asserted that Dai discloses a switching fabric that performs these steps by reading header information of the packet and disclosing a pointer register.

Applicants describe determining that the data includes a first line as determining whether the data includes the first line of data from the data packet supplied by the input port. (page 14, lines 20-29) If the data does include the first line, this indicates that the data has not previously been stored in the FIFO. Therefore, a location is allocated in the FIFO for the data and a pointer associated with the location in the FIFO is stored in the memory. (page 26, lines 3-9)

On the contrary, Dai merely describes reading a destination address included in the header information of each data packet received. Nowhere does Dai mention determining if the accepted data includes a first line of the data packet. Dai also fails to mention allocating a location in a FIFO for any type of data, let alone data accepted from a data packet that includes the first line of the data packet.

With reference to dependent claims 74-76, the applied references lack any teaching that would have suggested creating a pointer to a location allocated in the FIFO, and creating a tag identifying the data packet stored at the location in the FIFO. Furthermore, both Mann and Dai,

either singularly or in combination, fail to describe a method for a sink port in a cross-bar switch to collect data in a FIFO, as recited by Applicants' independent claim 71 from which claims 74-76 depend.

The Examiner correctly acknowledged that Mann fails to disclose creating a pointer to the location in the FIFO, and creating a tag identifying the data packet stored at the location in the FIFO. However, the Examiner asserted that Dai discloses a switching fabric that performs these steps by disclosing a pointer register and using the header information to route the data packet. As described above, Dai fails to mention allocating a location in a FIFO for any type of data, let alone data accepted from a data packet that includes the first line of the data packet. In addition, Dai never suggests creating a tag to identify the data packet. Contrary to the Examiner's assertion, routing a data packet based on header information does not equate to creating a tag that identifies a source of the data packet.

For at least these reasons, the Examiner has failed to establish a prima facie case for non-patentability of Applicant's claims 67-70 and 73-76 under 35 U.S.C. 103(a). Withdrawal of this rejection is requested.

Allowable Subject Matter

In the Office Action, the Examiner indicated that claims 77-79 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. For at least the reasons set forth above, Applicants' independent claim 71 is in condition for allowance. Consequently, dependent claims 77-79 are also in condition for allowance.

CONCLUSION

All claims in this application are in condition for allowance. Applicant respectfully requests reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 50-1778. The Examiner is invited to telephone the below-signed agent to discuss this application.

Date: Nov. 4, 2005

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